

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a Cu-based wiring layer containing a Cu-based metal as a main component and formed on a surface of a semiconductor substrate; and

an insulating layer formed to surround said Cu-based wiring layer;

wherein said Cu-based metal contains sulfur at a ratio ranging from  $10^{-3}$  atomic % to 1 atomic %.

2. The semiconductor device according to claim 1, wherein the content of sulfur in said Cu-based metal is in a range of  $10^{-2}$  atomic % to 1 atomic %.

3. The semiconductor device according to claim 1, wherein said Cu-based wiring layer is formed inside a wiring groove which is formed in said insulating layer.

4. The semiconductor device according to claim 3, wherein a conductive diffusion-prevention layer is formed on an inner surface of said wiring groove.

5. The semiconductor device according to claim 4, wherein said conductive diffusion-prevention layer contains one kind of material selected from the group consisting of Ta, TaN, Ti, TiN, WN, and TiSiN.

6. The semiconductor device according to claim 3, wherein an insulating diffusion-prevention layer is formed on an upper surface of said Cu-based wiring layer which is formed in said wiring groove.

7. The semiconductor device according to claim 6,

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wherein said insulating diffusion-prevention layer contains one kind of material selected from the group consisting of SiN, SiC, SiCO and SiCN.

8. The semiconductor device according to claim 3,  
5 wherein the content of sulfur in said insulating layer where said wiring groove is provided is in a range of 0 to 1 atomic %.

9. The semiconductor device according to claim 1,  
10 wherein a relative permittivity of said insulating layer is 3.0 or less.

10. The semiconductor device according to claim 1,  
wherein said Cu-based metal is Cu or a Cu alloy selected from the group consisting of Cu-Ag, Cu-Pt, Cu-Al, Cu-Co and Cu-C.

15 11. A semiconductor device comprising:

a Cu-based wiring layer containing a Cu-based metal as a main component and formed on a surface of a semiconductor substrate; and

20 an insulating layer formed to surround said Cu-based wiring layer;

wherein said Cu-based metal contains fluorine at a ratio ranging from  $10^{-3}$  atomic % to 1 atomic %.

12. The semiconductor device according to claim 11, wherein the content of fluorine in said  
25 Cu-based metal is in a range of  $10^{-2}$  atomic % to 1 atomic %.

13. The semiconductor device according to

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claim 11, wherein said Cu-based wiring layer is formed inside a wiring groove which is formed in said insulating layer.

14. The semiconductor device according to  
5 claim 13, wherein a conductive diffusion-prevention layer is formed on an inner surface of said wiring groove.

15. The semiconductor device according to  
10 claim 14, wherein said conductive diffusion-prevention layer contains one kind of material selected from the group consisting of Ta, TaN, Ti, TiN, WN, and TiSiN.

16. The semiconductor device according to  
15 claim 13, wherein an insulating diffusion-prevention layer is formed on an upper surface of said Cu-based wiring layer which is formed in said wiring groove.

17. The semiconductor device according to  
claim 16, wherein said insulating diffusion-prevention layer contains one kind of material selected from the group consisting of SiN, SiC, SiCO and SiCN.

20 18. The semiconductor device according to claim 13, wherein the content of fluorine in said insulating layer where said wiring groove is provided is in a range of 0 to 1 atomic %.

25 19. The semiconductor device according to claim 11, wherein a relative permittivity of said insulating layer is 3.0 or less.

20. The semiconductor device according to

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claim 11, wherein said Cu-based metal is Cu or a Cu alloy selected from the group consisting of Cu-Ag, Cu-Pt, Cu-Al, Cu-Co and Cu-C.

21. A method of manufacturing a semiconductor device, which comprises:

forming an insulating layer on a surface of a semiconductor substrate;

forming a wiring groove pattern in said insulating layer;

subjecting a resultant structure to a heat treatment in an inert atmosphere, in an atmosphere containing hydrogen or in a vacuum, to a plasma treatment in an atmosphere containing ammonia, or to a treatment using an ammonia solution;

forming a conductive diffusion-prevention layer on an inner surface of said wiring groove that has been subjected to any of the aforementioned treatments and on a surface of said insulating layer that has been subjected to any of aforementioned treatments;

forming a Cu-based metal layer on a surface of said conductive diffusion-prevention layer thereby to bury said wiring groove with a Cu-based metal;

selectively removing portions of the Cu-based metal layer and of said conductive diffusion-prevention layer, which are deposited on regions other than the inner surface of said wiring groove thereby to form a Cu-based wiring layer inside said wiring groove; and

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forming an insulating film which is capable of suppressing the diffusion of Cu-based metal on a surface of said Cu-based wiring layer and on a surface of said insulating layer;

5            wherein said Cu-based metal contains sulfur or fluorine at a ratio ranging from  $10^{-3}$  atomic % to 1 atomic %.

10           22. The method according to claim 21, wherein the content of sulfur or fluorine in said Cu-based metal is in a range of  $10^{-2}$  atomic % to 1 atomic %.

15           23. The method according to claim 21, wherein the content of sulfur or fluorine in said insulating layer which has been subjected to any of the aforementioned treatments is in a range of 0 to 1 atomic %.

20           24. The method according to claim 21, wherein the temperature of said heat treatment is in a range of 200 to 500°C.

25           25. A method of manufacturing a semiconductor device, which comprises:

             forming an insulating layer on a surface of a semiconductor substrate;

             forming a wiring groove pattern in said insulating layer;

             forming a conductive diffusion-prevention layer on an inner surface of said wiring groove and on a surface of said insulating layer;

             forming a Cu-based metal layer on a surface of

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said conductive diffusion-prevention layer thereby to bury said wiring groove with a Cu-based metal;

subjecting a resultant structure to a heat treatment in an inert atmosphere, in an atmosphere containing hydrogen or in a vacuum;

selectively removing portions of Cu-based metal layer and of said conductive diffusion-prevention layer, which are deposited on regions other than the inner surface of said wiring groove thereby to form a Cu-based wiring layer inside said wiring groove; and

forming an insulating film which is capable of suppressing the diffusion of Cu-based metal on a surface of said Cu-based wiring layer and on a surface of said insulating layer;

wherein said Cu-based metal contains sulfur at a ratio ranging from  $10^{-3}$  atomic % to 1 atomic %.

26. The method according to claim 25, wherein the content of sulfur in said Cu-based metal is in a range of  $10^{-2}$  atomic % to 1 atomic %.

27. The method according to claim 25, wherein the content of sulfur in said insulating layer which has been subjected to any of the aforementioned treatments is in a range of 0 to 1 atomic %.

28. The method according to claim 25, wherein the temperature of said heat treatment is in a range of 200 to 500°C.

29. A method of manufacturing a semiconductor

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device, which comprises:

forming an insulating layer on a surface of  
a semiconductor substrate;

5 forming a wiring groove pattern in said insulating  
layer;

forming a conductive diffusion-prevention layer on  
an inner surface of said wiring groove and on a surface  
of said insulating layer;

10 forming a Cu-based metal layer on a surface of  
said conductive diffusion-prevention layer thereby to  
bury said wiring groove with a Cu-based metal;

15 selectively removing portions of the Cu-based  
metal layer and of said conductive diffusion-prevention  
layer, which are deposited on regions other than the  
inner surface of said wiring groove thereby to form  
a Cu-based wiring layer inside said wiring groove;

20 subjecting a resultant structure having said  
Cu-based wiring layer formed therein to a heat  
treatment in an inert atmosphere, in an atmosphere  
containing hydrogen or in a vacuum, to a plasma  
treatment in an atmosphere containing ammonia, or to  
a treatment using an ammonia solution; and

25 forming an insulating diffusion-prevention layer  
which is capable of suppressing the diffusion of  
Cu-based metal on a surface of said Cu-based wiring  
layer and on a surface of said insulating layer;

wherein said Cu-based metal contains sulfur or

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fluorine at a ratio ranging from  $10^{-3}$  atomic % to 1 atomic %.

30. The method according to claim 29, wherein the content of sulfur or fluorine in said Cu-based metal is in a range of  $10^{-2}$  atomic % to 1 atomic %.

31. The method according to claim 29, wherein the content of sulfur or fluorine in said insulating layer which has been subjected to any of the aforementioned treatments is in a range of 0 to 1 atomic %.

32. The method according to claim 29, wherein the temperature of said heat treatment is in a range of 200 to 500°C.

33. A method of manufacturing a semiconductor device, which comprises:

forming an insulating layer on a surface of a semiconductor substrate;

forming a wiring groove pattern in said insulating layer;

subjecting a resultant structure to a heat treatment in an inert atmosphere, in an atmosphere containing hydrogen or in a vacuum, to a plasma treatment in an atmosphere containing ammonia, or to a treatment using an ammonia solution;

forming a conductive diffusion-prevention layer on an inner surface of said wiring groove and on a surface of said insulating layer;

forming a Cu-based metal layer on a surface of

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said conductive diffusion-prevention layer thereby to bury said wiring groove with a Cu-based metal;

5       subjecting said Cu-based metal layer to a heat treatment in an inert atmosphere, in an atmosphere containing hydrogen or in a vacuum;

10       selectively removing portions of the Cu-based metal layer and of said conductive diffusion-prevention layer, which are deposited on regions other than the inner surface of said wiring groove thereby to form a Cu-based wiring layer inside said wiring groove;

15       subjecting a resultant structure having said Cu-based wiring layer formed therein to a heat treatment in an inert atmosphere, in an atmosphere containing hydrogen or in a vacuum, to a plasma treatment in an atmosphere containing ammonia, or to a treatment using an ammonia solution; and

20       forming an insulating diffusion-prevention layer which is capable of suppressing the diffusion of Cu-based metal on a surface of said Cu-based wiring layer and on a surface of said insulating layer;

      wherein said Cu-based metal contains sulfur or fluorine at a ratio ranging from  $10^{-3}$  atomic % to 1 atomic %.

25       34. The method according to claim 33, wherein the content of sulfur or fluorine in said Cu-based metal is in a range of  $10^{-2}$  atomic % to 1 atomic %.

      35. The method according to claim 33, wherein the

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content of sulfur or fluorine in said insulating layer which has been subjected to any of the aforementioned treatments is in a range of 0 to 1 atomic %.

36. The method according to claim 33, wherein the  
5 temperature of said heat treatment is in a range of 200 to 500°C.

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